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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 07/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/721,310	IWASAKI, GO	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 13-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,8 and 13-16* is/are rejected.

7)☒ Claim(s) *3-7,9,10 and 17-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on 05/02/2006 has been entered.

2. Claims 1-10,13-19 are presented for examination.

Response to Arguments

3. Applicant's arguments with respect to claims 1-10,13-19 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 13-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Houghton et al. (U.S. Patent No. 5,355,029).

Regarding claim 13, Houghton et al. disclose an output buffer circuit (Figure 2) comprising:

a plurality of unit circuits (Figure 2, 16) in each of which a pull-up transistor (Figure 2, P18) controlled by a first input signal (Figure 2, a signal from p10) is connected between a high-potential power supply (Figure 2, VDD) and common node (Figure 2, OUT) , and a pull-down transistor (Figure 2, P19) controlled by a second input signal (Figure 2, signal from P13) is connected between said common node (Figure 2, OUT) and a low-potential power supply (Figure 2, VSS); and

an output terminal (Figure 2, OUT) connected to a common connecting point of said common nodes of said plurality of unit circuits (Figure 2, Figure 1, OUT); and

resistors (Figure 2, R2, R3) formed respectively between said pull-up transistor and common node and between said common node and pull-down transistor in each of said unit circuits.

Regarding claim 14, Houghton et al. disclose wherein the resistors formed respectively between the pull-up transistor and common node and between common node and pull-down transistors have the same resistance (Figure 2, R2, R3 is 70).

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 1-2,8 are rejected under 35 U.S.C. 102(e) as being anticipated by Kurisu et al. (Pub. U.S. Patent No. 2002/0030517).

Regarding claims 1-2, Kurisu et al. disclose an output buffer circuit (Figure 5) comprising:

a plurality of unit circuits (Figure 5 B20) in each of which a pull-up transistor (Figure 5, P3) controlled by a first input signal (Figure 5, signal TS go through INV3) is connected between a high-potential power supply (Figure 5, VDD) and common node (Figure 5) , and a first pull-down transistor (Figure 5, N2) controlled by a second input signal (Figure 5, signal from TB) and a second pull-down transistor (Figure 5, N3) controlled by a third input signal (Figure 5, signal from TS) are connected in series between said common node (Figure 5, N2 and N3 in series) and a low-potential power supply (Figure 5, VSS, [0014]);

an output terminal (Figure 5, TRV) connected to a common connecting point (Figure 5, TOUT) of said common nodes of said plurality of unit circuits (Figure 5); and

first resistors (Figure 5, L, [0062], impedance of L) formed respectively between said common nodes of said plurality of unit circuits and said common connecting point (Figure 5).

(L is a resistor (a impedance is defined in [0062]), or reference U.S. 6,204,692, Nakagawa defined transmission line by means of resistors in column 10 lines 12-13. L is a impedance of resistors in transmission line from TOUT to TRV).

Regarding claim 8, Kurisu et al disclose wherein each of said pull-up and pull-down transistors is a MIS transistor (Figure 5, P3, N2).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurisu et al (Pub. U.S. 2002/0030517) in view of Kohno (U.S. Patent No. 6,041,013).

Regarding claims15-16, Kurisu et al. disclose a semiconductor memory (Figure 6) comprising:

a plurality of memory cells (a plurality of memory cells is seen to be inherent in the prior art memory device) ;

a plurality of terminals (Figure 6, B20, B21) including an output terminal (Figure 6, TOUT); and

said output buffer circuit (Figure 6) comprising a plurality of unit circuits (Figure 6, B20,B21) in each of which a pull-up transistor (P3) controlled by a first input signal (TS1 through INV3) is connected between a high-potential power supply (VD) and common node (Figure 6) and a pull-down transistor (Figure 6, N3) controlled by a second input signal (Figure6, TS1) is connected between said common node and a low-potential power supply (Figure 6, VSS) , and comprising first resistors (Figure 6, L, as described in claim 1) connected respectively between said common nodes of said plurality of unit circuits and a common connecting point (Figure 6, TOUT) of said common nodes, and wherein said first resistors are formed between said output buffer circuit and output terminal (Figure 6, impedance I resistor is between common node TOUT and output TRV).

Kurisu et al. as described above, fails to disclose arrangement of position of an output buffer circuit is positioned adjacent to the memory cell. However, Kohno discloses an output buffer is positioned adjacent the memory cell in Figure 2, 30-B1-30B8 or in Figure 8, output buffer 32-An is adjacent to memory cell.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to arrange the output buffer circuit in position of adjacent to memory cell. Applicant has not disclosed that output buffer circuit positioned adjacent to memory cell provides an advantage, is used for particular purpose, or solves a state problem.

Therefore, it would have been obvious to a person of ordinary skill in this art to modify the location of output buffer circuit in Kohno to obtain the invention as specified in claim 15.

Allowable Subject Matter

9. Claims 3-7, 9-10, 17-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3-7,9-10, 17-19 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Houghton et al. (U.S. Patent No. 5,355,029), Kurisu et al. (Pub. U.s. Patent No. 2002/0030517), Kohno (U.S. Patent No. 6,041,013), and others, does not teach the claimed invention having a second resistors are arranged as

in claims 3-7, and the structure of transistors and resistor as claims 9-10 disclosed, and wherein if the number of said first resistors is an even number, said first resistors are symmetrically arranged with respect to a central line of said output buffer circuit and output terminal, and have the same value, the same size, and the same shape as claim 17 disclosed, and wherein said first resistors are formed on at least not less than one of three sides of said output terminal, which do not oppose said output buffer circuit as claims 18-19 disclosed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thong Q. Le
Primary Examiner
Art Unit 2827

7/9/2006